This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2873188, IEEE Transactions on Power Electronics

A Novel Nine-Level Quadruple Boost Inverter with Inductive-load Ability

Junfeng Liu, Weijie Lin, Jialei Wu, Jun Zeng

***Abstract*—a novel single phase nine-level switched-capacitor inverter (9LSCI) is presented with quadruple boost ability and reduced components. The proposed topology with single dc source employs only eight switches to realize nine-level output, self-voltage balance of capacitors, quadruple boost and inductive-load ability, thus, the effective cost is cut down compared to other switched-capacitor multilevel inverters (SCMLIs). Different from other SCMLIs, the proposed 9LSCI has no need for backend H-bridge, of which four switches need to withstand the peak voltage of output. Hence, total standing voltage (TSV) can be reduced. The operation principles containing the self-voltage balance of capacitors are described in detail. The quantitative comparisons, modified cost function (CF), as well as the loss evaluations are examined in depth. Finally, multicarrier phase disposition (PD) PWM method is adopted and a laboratory prototype is implemented with the rated output of 220V-500W. The experimental results also verify the feasibility of the proposed topology.**

***Index Terms*—Nine-level switched-capacitor inverter (9LSCI), quadruple boost, multilevel inverters, self-voltage balance.**

I. Introduction

Multilevel inverters (MLIs) have been studies during recent years and regarded as key solutions for high-voltage or high-power applications of renewable energy generation (REG) field [1]-[3]. The main advantages of MLIs are output improvement with low voltage harmonic, reduced voltage stress on switches, low *dv*/*dt* stress, less requirement for filters, and high modularity [4].

There are three types of conventional multilevel topologies: neutral-point-clamped (NPC) topology, flying capacitor (FC) topology, and cascaded H-bridge (CHB) topology. However, the electric energy from renewable energy sources, such as photovoltaic (PV) arrays and fuel cells, are largely in the form of low voltage [5], which need to be transformed to higher ac voltage. One of the traditional solutions is to cascade a frontend dc-dc boost converter with a backend conventional MLI [6]. Furthermore, auxiliary balance circuits, current and voltage sensors, or complicated control algorithms is needed for keeping the capacitors' voltage balance of NPC and FC topologies. All of these lead to additional complexity and reduced efficiency.

Alternatively, switched-capacitor multilevel inverter (SCMLI) has been extensively investigated as a new approach to solve aforementioned issues. Hereby, a multilevel boost inverter based on switched-capacitor structure was presented in [7], contributing to produce seven levels with less components compared with conventional topologies, while it has no inductive-load ability. The topology integrating a T-type structure was proposed with nine-level voltage in [8], of which the switched-capacitor cell can maintain the voltage balance without any sensors. However, it needs two symmetrical dc sources to regulate the voltage for the clamping capacitors of dc side. And importantly, it has no boost ability. On the other hand, two types of nine-level SCMLIs with single dc source were proposed in [9] and [10], respectively. Both of them can get the voltage balance of capacitors without auxiliary methods. But nonetheless, both have poor boost ability.

Typically, the SCMLI topologies with the capability to extend output levels were proposed successively. Most have considerable boost ability [11]-[13], while another proposed in [14] does not. Anyhow, a great number of switching devices are employed in the output current paths of this kind of topologies, resulting in lower efficiency. All the SCMLIs aforementioned require a backend H-bridge for polarity change, in which four high blocking-voltage switches must withstand the peak voltage of output. Conversely, a SCMLI with less blocking voltage was proposed in [15] and had no need for backend H-bridge, while too much switches are needed. Furthermore, some SCMLI topologies are suggested to operate in the cascaded connection for more voltage levels [16], [17]. However, multiple isolated dc sources are needed.

This paper presents a nine-level switched-capacitor inverter (9LSCI) with quadruple boost ability and reduced components. The circuit configurations, operation principles, as well as the self-voltage balance of capacitors are examined in detail in Section II. The modulation analysis and capacitance calculation are conducted in Section III. The comparative study against other existing topologies is carried out in Section IV based on reasonable conditions and the modified cost function. In Section V, a laboratory prototype with rated 220V_{rms}-500W output is implemented and the experimental analysis is given to verify the performance. Finally, the conclusions are presented in Section VI.

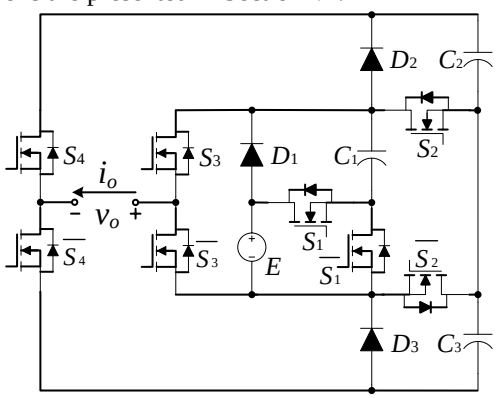

Fig. 1. Circuit topology of the proposed 9LSCI

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2873188, IEEE Transactions on Power Electronics

II. Proposed 9LSCI Topology

A. Circuit Topology and Operation Principles

Fig.1 demonstrates the circuit topology of the proposed 9LSCI. It comprises one dc source, three capacitors, three power diodes, and only eight power switches. To achieve nine-level output and quadruple boost, the capacitor C_1 and C_2/C_3 are expected to be charged on V_{dc} and $2V_{dc}$, respectively.

The current flowing paths and the states of switches at each level are shown in Fig. 2 and Table I, respectively. Particularly, the switch S_i has complementary operation with $\overline{S_i}$ (i = 1, 2, 3, 4), which means less complexity of control for the proposed 9LSCI. Thus, only four switches' states are listed in Table I for a simplified view. Both S_4 and $\overline{S_4}$ operate at the fundamental frequency to reduce switching loss. The reverse current paths for inductive load (blue line) can be obtained from Fig.2, and meanwhile, the output levels keep the same with that for resistant load. The voltage ratings of S_3 and $\overline{S_3}$ are the half of total output, thus, no backend H-bridge is needed for the proposed 9LSCI.

TABLE I
The Switching States of the Proposed 9LSCI at Each Level

Output level ($\times V_{dc}$)	+4	+3	+2	+1	+0	-0	-1	-2	-3	-4
S_1	1	0	1	0	1	1	0	1	0	1
S_2	0	0	1	1	1	0	0	0	1	1
S_3	1	1	1	0	0	1	1	0	0	0
S_4	0	0	0	0	0	1	1	1	1	1

*1 or 0: for the switch is ON or OFF, respectively

B. Self-voltage Balance of the capacitors

The series-parallel technique is used to achieve self-voltage balance of capacitors [13]. As shown in Fig.2 (c), (d), (g), and (h), the capacitor C_1 is in parallel with dc source and charged to the voltage V_{dc} when the switch $\overline{S_1}$ is turned on during the levels of $\pm V_{dc}$ and $\pm 3V_{dc}$,. Conversely, the pre-charged capacitor C_1 is in series connection with dc source when the switch S_1 is turned on while the diode D_1 becomes reverse biased, so that C_1 and dc source are able to output in series, having the total amplitude of $2V_{dc}$. As shown in Fig.2 (a), (e), and (j), the capacitors C_3 is in parallel with a $2V_{dc}$ dc source equivalently and charged on $2V_{dc}$ (the capacitor C_2 works in the similar way in a cycle) when the switch S_2 is also turned on during levels of +0, $+2V_{dc}$, or $-4V_{dc}$, respectively. Considering the total parasitic resistance R_{Charge} and the time constant $R_{Charge}\cdot C_i$ of the charging loops are both relatively low, the time duration for capacitors to be fully replenished can get guaranteed compared with the duration of each voltage level.

When the fully replenished capacitors discharge and pump the internal stored energy to load for producing more voltage levels, the voltages are reduced from their expected value (V_{dc} or $2V_{dc}$) until the coming of the next charging period. Therefore, voltage ripples appear on the capacitors C_1-C_3. Taking the discharging durations of C_1-C_3 and the load current at each level into consideration, the appropriate capacitance can be calculated and selected. Therefore, the voltage ripples of capacitors can be limited within the allowable range. The detailed capacitance calculations are given in Section III.

Hence, the capacitors C_1, C_2, and C_3 are charged several times in a cycle and their voltages maintain at V_{dc}, $2V_{dc}$, and $2V_{dc}$ respectively without any auxiliary balance circuits and complicated control strategy. This feature of the proposed 9LSCI can further reduce the complexity of control compared with the conventional topologies.

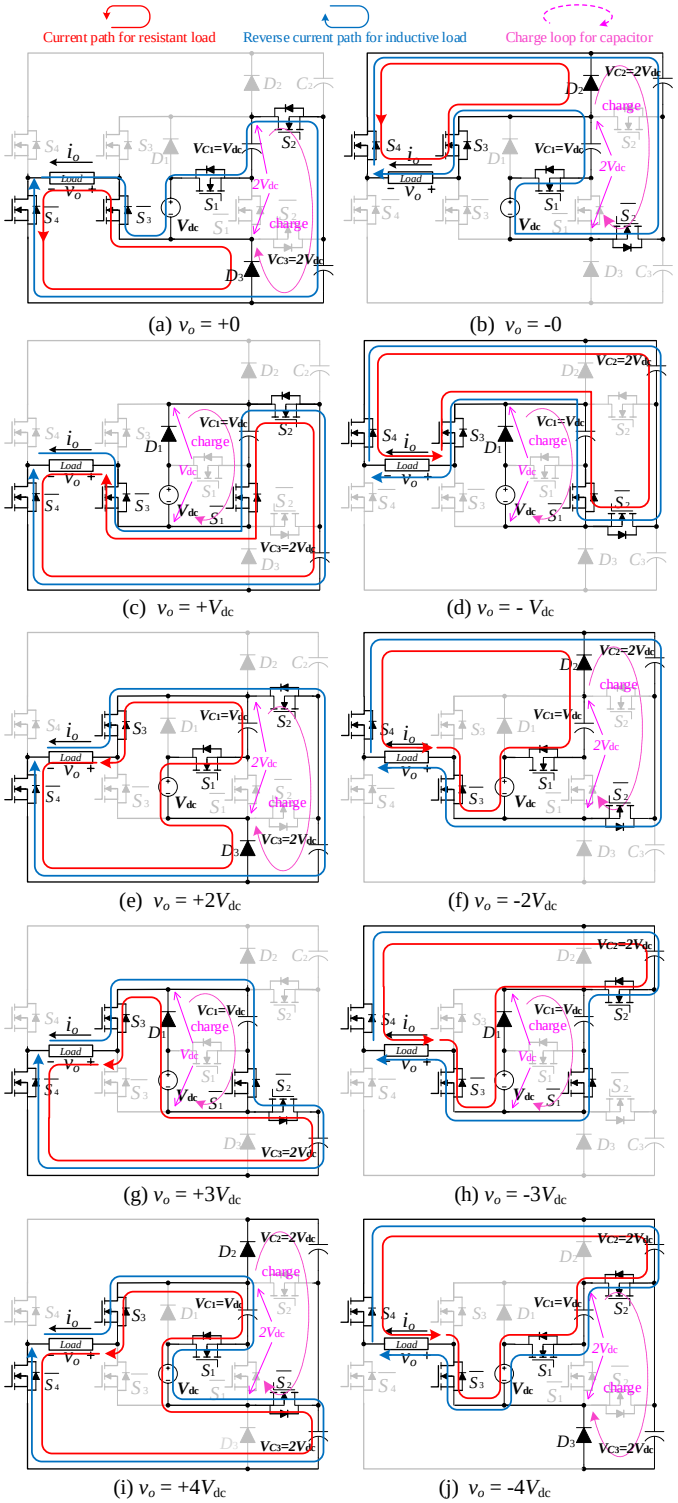

Fig. 2. Current flowing paths and components states at different voltage levels.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2873188, IEEE Transactions on Power Electronics

III. Modulation and Capacitance Analysis

A. Modulation Strategy for the Proposed 9LSCI

The optimized multicarrier phase disposition (PD) PWM method is a widely-used control strategy for MLI [11], and is adopted for the proposed topology. As depicted in Fig.3(a), four groups of triangle carriers v_{t1}-v_{t4} with the same frequency, phase, and amplitude are disposed from top to bottom in sequence, comparing with the sinusoidal waveform v_m. Fig.3(b) demonstrates the modulation logic based on the comparison results of multicarrier PD method. According to Table I, the simple logic circuits or a look-up table method of the controller can be used for the PWM signals of the switches.

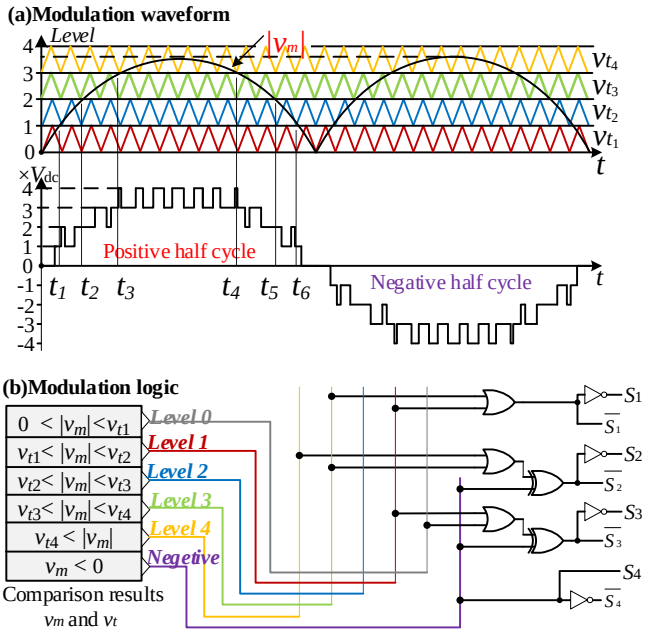

Fig. 3. PD PWM modulation strategy and logic for the proposed topology

B. Capacitance Calculation

The maximum voltage ripple (or lowest voltage amplitude) over each capacitor occurs during the largest discharging gap for pumping the stored energy to load side in a cycle. Assuming the load is pure resistant, the continuous discharging amount of C_i during its largest discharging gap $[t_{x\_i}, t_{y\_i}]$ can be calculated as:

$$\Delta Q_i = \int_{t_{x\_i}}^{t_{y\_i}} \sqrt{2} I_{load} \sin \omega t dt \tag{1}$$

Therefore, the capacitance of C_i should satisfy

$$C_i > \frac{1}{\Delta V_{ripple}} \int_{t_{x\_i}}^{t_{y\_i}} \sqrt{2} I_{load} \sin \omega t dt \tag{2}$$

where ΔV_{ripple} and I_{load} represent the allowable voltage ripple over the capacitor C_i and the load current across it, respectively. Combining Fig.2 and Fig.3(a), it is obvious that the largest discharging gap for C_1 is $[t_3, t_4]$ outputting the fourth level, and that for C_3 is $[t_2, t_5]$ outputting the third and fourth levels. C_2 has the same capacitance as C_3 due to the similar operational method. In view of 5%-10% allowable voltage ripple over capacitors [9], [10], the capacitance can be determined finally.

IV. Comparative Study with Other MLIs

In order to evaluate the pros and cons of the proposed 9LSCI, a comprehensive comparative study is conducted in this section. For fair comparisons here, the SCMLIs and conventional topologies taken into comparison are expected to have the same output voltage levels with only single dc source. The comparative study is divided into two aspects.

A. Quantitative Comparisons and Cost Function Evaluation against Other SCMLIs

The results of quantitative comparison for component count and total standing voltage (TSV) are listed in Table II. TSV can reflect the total voltage rating of the switching semiconductor devices in a topology, and is defined as

$$TSV = \frac{\sum_{i=1}^{n} V_{b\_sw,i} + \sum_{j=1}^{m} V_{b\_d,j}}{V_{o\_\max}} \tag{3}$$

where $V_{b\_sw,i}$, and $V_{b\_d,i}$ represent the maximum blocking voltage of each switch and diode in the topology, respectively. V_{o_max} is the maximum output peak voltage.

One important proviso is that the SCMLI proposed in [12] employs lot of diodes rather than power switches for more voltage levels, thus, it has no inductive-load ability. Therefore, the proposed 9LSCI topology requires the least number of power switches among the compared SCMLIs with inductive-load ability. Furthermore, the drivers with isolated dc sources and other peripheral components are saved as well. It is obviously that both the proposed topology and that in [14] have no need for the backend H-bridge withstanding the total voltage of output and have the lowest TSV. That is to say, the high withstand-voltage switches can be reduced. The TSV of the SCMLI in [14] is lower than that of the proposed 9LSCI, however, up to nineteen switches are required in [14]. Thereby, a great number of switches are sacrificed for TSV.

In order to evaluate the different SCMLIs, a proportion of cost function (CF) equation is suggested based on component count and TSV [10]. Furthermore, the modified CF equation combined with boost ability is examined in this paper for the SCMLIs with the same voltage levels and single dc source:

$$CF = N_{switch} + N_{driver} + N_{diode} + N_{cap} + \frac{\alpha \times TSV}{Gain} \tag{4}$$

α is a weight coefficient to measure the importance between component count and TSV, and it is set to 1.0 here. *Gain* represents the voltage boosting factor of SCMLIs. As shown in Table II, the proposed 9LSCI has the lowest value of CF compared to other SCMLIs, which demonstrates the merits of the proposed topology from a comprehensive viewpoint with respect to components number, boost ability, and TSV.

B. Quantitative Comparisons and Loss Evaluation against Conventional MLI Topologies

The results of quantitative comparisons and loss evaluation against conventional MLI topologies with single dc source are shown in Table III. It is obvious that the NPC and FC topologies employ much more components for the same output levels compared with the proposed 9LSCI.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2873188, IEEE Transactions on Power Electronics

TABLE II
QUANTITATIVE COMPARISON AND COST FUNCTION EVALUATION FOR 9-L SCIMLI WITH SINGLE DC SOURCE

Ref.	N_{switch}	N_{driver}	N_{diode}	N_{cap}	TSV	*Gain*	H-bridge needed	Inductive-load ability	CF
[9]	9	9	2	2	6.5	2	Yes	Yes	25.25
[10]	10	8	1	2	6	2	Yes	Yes	24.00
[11]	13	13	0	3	6.25	4	Yes	Yes	30.56
[12]	8	8	6	3	8	4	Yes	No	37.00
[13]	10	10	3	3	6.25	4	Yes	Yes	27.56
[14]	19	19	3	3	4.75	4	No	Yes	45.18
[15]	10	10	4	4	7.75	1	Yes	Yes	35.75
Proposed	8	8	3	3	5.75	4	No	Yes	23.43

TABLE III
QUANTITATIVE COMPARISON AND LOSS EVALUATION AGAINST 9-LEVEL CONVENTIONAL MLIS WITH PURE RESISTANT LOAD

9-level MLI topologies	Voltage balance of Capacitors	*Gain*	Total number of devices			Conducting devices		Switching transitions
			N_{switch}	N_{diode}	N_{cap}	N_{sem}	N_{cap}	
NPC	Auxiliary method	1	16	14	8	8	4(max)	2
FC	Auxiliary method	1	16	0	9	8	8(max)	2
Proposed	Self-balance	4	8	3	3	3 - 4	2(max)	2 - 4

* ***Total number of devices***: indicating the total number of devices employed in 9L MLIs.
Conducting devices: indicating the number of conducting devices in the output current path for load at each level.
Switching transitions: indicating the number of the power switches which need to turn on/off when the output level changes once.
N_{switch}, N_{driver}, N_{diode}, N_{cap}, **and** N_{sem} : the number of switches, drivers, diodes, capacitors, and semiconductor devices including switches and diodes respectively.

Hereby, conduction and switching losses are taken into consideration for the conventional topologies. The conduction loss is mostly caused by the parasitic parameters (including the on-state resistances and forward voltage drops of devices) in the output current paths. Assuming pure resistant load is applied, the number of conducting devices in output current path at each level for NPC and FC topologies is more than double that for the proposed 9LSCI from Table III, which means much higher conduction loss and reduced efficiency.

The switching loss is directly related to the parasitic capacitor C_p of switches [12], and can be calculated as:

$$P_{sw\_loss} = f_{sw} C_p V_b^2 \quad (3)$$

where f_{sw} and V_b are switching frequency and blocking voltage of the switch, respectively.

The blocking voltage of each switch in NPC and FC topologies is indeed lower because much more switches, capacitors and diodes are employed to divide and clamp the total voltage. However, as mentioned above, the essential auxiliary methods of the capacitors' voltage balancing and the cascaded connection of frontend boost converter unavoidably lead to more switching loss and reduced efficiency for NPC and FC topologies. Rather, the feature of boost ability and relatively numerous levels with self-voltage balance allows the proposed topology to operate at lower switching frequency. Thus, the efficiency and lifetime can improve for capacitors.

V. EXPERIMENTAL RESULTS

A 220V-500W experimental prototype as shown in Fig. 4(a) is implemented to verify the proposed 9LSCI. The devices employed in the experiment prototype are demonstrated in Table IV. The output frequency and carrier frequency are set to 50Hz and 4kHz respectively based on the modulation analysis in section III. The maximum input voltage is 80V.

The experimental waveforms are shown in Fig.4(b)-(f). It can be observed from Fig.4(b) that the output waveforms contain nine steady levels and the peak value of output voltage reaches 320V with the input of 80V, thus, verifying the quadruple boost ability of the proposed 9LSCI. The efficiency is more than 93% with the rated output of 220Vrms-500W. On the other hand, the inductive load is applied as shown in Fig. 4(c), and the THD of output current is 1.8%. The inductive-load ability of the proposed topology is testified.

TABLE IV
THE DEVICES EMPLOYED IN THE EXPERIMENT

Devices	Type	Parameter	Amount
Power MOSFETs	IRFP243	150V/17A	2
	IRFP245	250V/14A	4
	IRFP443	450V/7A	2
Ultrafast rectifier	STPS16150	150V/16A	1
	STTH1003	300V/10A	2
Electrolytic capacitor	3300μF	100V	1
	3300μF	200V	2

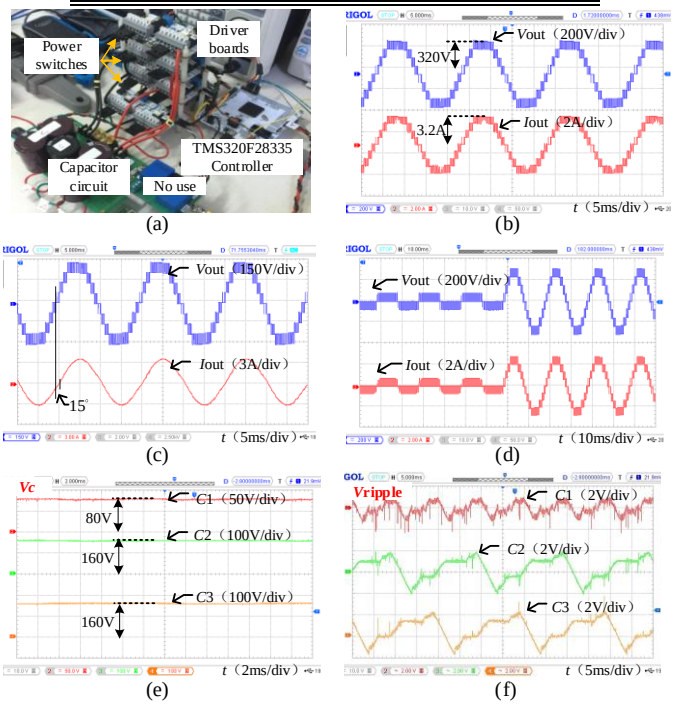

Fig. 4. (a) Experimental prototype. (b) Output voltage and current waveforms with pure resistive load of 100Ω. (c) Output with inductive load of 80Ω and 56mH. (d) Output waveforms within a change from 10Vrms to 220Vrms. (e) Voltages over the capacitors. (f) Voltage ripples over the capacitors.

Moreover, all the capacitors can maintain on their expected voltage and the voltage ripples over them are less than 2.5% as shown in Fig. 4(e) and (f) respectively, which means lower capacitance can be selected. So that the parallel-connected polypropylene film capacitors with better high-frequency performance and reliability can be applied for practical applications. The self-voltage balance of capacitors is verified with good precision. To further observe the instantaneous output performance, the experimental waveforms of a sudden output change from 10V to 220V realized by controller are shown in Fig. 4(d). It is evident that the proposed 9LSCI can operates well for dramatic increase of output power. Consequently, the quadruple boost and inductive-load ability, nine-level output, and self-voltage balance of capacitors have been validated for the proposed 9LSCI.

VI. Conclusions

This paper proposes a 9LSCI with the features of quadruple boost, reduced components, self-voltage balance, and inductive-load ability. The proposed topology employs only eight switches and has no need for the backend H-bridge. The results of comparisons against other topologies demonstrate its merits from a comprehensive viewpoint. Finally, the prototype experiment with multicarrier PD PWM method is implemented to further verify the feasibility.

VII. Acknowledgements

The authors gratefully acknowledge the financial support the financial support of National Natural Science Foundation of China (No. 61573155, 51877085), Guangdong Natural Science Foundation (No.2016A030313508), Guangdong Science and Technology Planning (No.2016A010102007).

References

[1] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—state of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[2] H. Akagi and R. Kondo, "A transformerless hybrid active filter using a three-level pulsewidth modulation (PWM) converter for a medium-voltage moter drive," *IEEE Trans. Power Electron*., vol.25, no. 6, pp. 1365-1374, Jun. 2010.

[3] G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phase grid-connected converter for renewable distributed systems," *IEEE Trans. Ind. Electron*., vol. 60, no. 3, pp. 906–918, Mar. 2013.

[4] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[5] S. B. Kjaer, J. K. Pedersen and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl*., vol. 41, no. 5, pp. 1292–1306, September/October 2005.

[6] T. Kerekes, D. Séra, and L. Máthé, "Three-phase photovoltaic systems: structures, topologies, and control," *Electr. Power Compon. Syst*., vol. 43, no. 12, pp. 1364–1375, July 2015.

[7] S. H. Hosseini, A. Z. Gharehkoushan and H. Tarzamni, "A multilevel boost converter based on a switched-capacitor structure," *2017 10th International Conference on Electrical and Electronics Engineering (ELECO)*, Bursa, 2017, pp. 249-253.

[8] N. Sandeep and U. R. Yaragatti, "A switched-capacitor-based multilevel inverter topology with reduced components," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5538–5542, July 2018.

[9] J. Liu, J. Wu, J. Zeng, and H. Guo H, "A novel nine-level inverter employing one voltage source and reduced components as high-frequency ac power source," *IEEE Trans. Power Electron*., vol. 32, no. 4, pp. 2939-2947, April 2017.

[10] R. Barzegarkhoo, M. Moradzadeh, and F. Blaabjerg, "A new boost switched-capacitor multilevel converter with reduced circuit devices," *IEEE Trans. Power Electron*., vol. 33, no. 8, pp. 6738-6754, Aug 2018.

[11] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, February 2012.

[12] Y. Ye, K. W. E. Cheng, J. Liu and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron*., vol. 61, no. 12, pp. 6672-6680, December 2014.

[13] E. Babaei, and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron*., vol. 61, no. 9, pp. 4614–4621, September 2014.

[14] A. Taghvaie, J. Adabi and M. Rezanejad, "A Self-Balanced Step-Up Multilevel Inverter Based on Switched-Capacitor Structure," *IEEE Trans. Power Electron*, vol. 33, no. 1, pp. 199-209, Jan 2018.

[15] J. Zeng, J. Wu, J. Liu, and H. Guo, "A quasi-resonant switched-capacitor multilevel inverter with self-voltage balancing for single-phase high-frequency ac microgrids.*IEEE Trans. Ind. Informat*., vol. 13, no. 5, pp. 2669-2679, Oct 2017.

[16] R. Barzegarkhoo, H. M. Kojabadi, and L. Chang, "Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple DC link producer with reduced number of switches," *IEEE Trans. Power Electron*., vol. 31, no. 8, pp. 5604-5617. August 2016.

[17] J. Liu, K. W. E. Cheng, and Y. Ye, "A cascade multilevel inverter based on switched-capacitor for high-frequency ac power distribution system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4219-4230, August 2014.